Gate Oxide Breakdown on Low Noise and Power Amplifier Performance

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Abstract — **This paper, for the first time, studies the influence nMOSFET gate oxide breakdown (BD) has on the performance of CMOS low noise amplifiers (LNA) and power amplifiers (PA) using an equivalent RF circuit model. Cascode LNAs are found to be more reliable than common source LNAs in terms of gate oxide reliability. It is shown for a Class-E PA oxide breakdown effects lead to an increase in the switching transistor's "on" voltage, which, in turn leads to substantial decreases in the output power and drain efficiency.**

I. Introduction

Gate oxide breakdown has been studied extensively over the past few years and many efforts that investigate the defect generation leading to breakdown and the nature of the conduction after breakdown have been presented. Recent research concerning the impact MOSFET gate oxide breakdown has on circuits has been reported in [1,2,3,4,5]. In [4] it was demonstrated that a nonzero probability that digital circuits would remain functional beyond the first gate oxide hard breakdown exists, and an equivalent circuit was proposed to describe the gate current in an nMOSFET after gate oxide breakdown. In [5] an equivalent RF circuit model for MOSFETs after gate oxide breakdown has been proposed. In this paper, the effect of gate oxide breakdown location on circuit performance is examined using the equivalent model.

II. Experiments

The devices used in this work are fabricated with a 1.5 V, 0.16 μm CMOS technology with channel length L = 0.16 μm and channel width W = 10 μm. The oxide thickness t_{ox} is 24 Å. The devices are tested with Cascade probe station, Agilent 4156B Precision Semiconductor Parameter Analyzer and Agilent 8510C Network Analyzer.

The stress condition is set at constant gate voltage of 4.5 V and constant drain voltage of 2 V with the source and the substrate grounded. The stress automatically stops when a threshold gate current of 1 mA is met. After breakdown, S-parameters and $I - V$ curves including $I_g - V_g$ are then measured, and the BSIM3V3 model as well as other parameters are extracted.

III. Equivalent RF Circuit Model of a MOSFET After Gate Oxide Breakdown

The modified equivalent circuit, which aims at RF applications, is shown in Fig. 1. A resistor can be thought of to exist in the channel. Due to the breakdown position variation, the breakdown path resistor R_{path} connects to any point of the channel resistor. Thus, the drain, gate and source form a star network, which can be transformed into a delta network. This is the origin of R_{gd} and R_{gs}. Due to the magnitude of the channel resistance and breakdown path resistance, channel resistance value remains roughly unchanged after the network transformation, therefore the transistor needs no modification. So with different values of R_{gd} and R_{gs} representing the conducting path from gate to drain, from gate to source, or from gate to both drain and source [6], the gate-to-channel or gate-to-extension breakdown can be distinguished and modeled. R_g and the RC network between the drain, source and substrate is for more accurate RF modeling [6,7,8].

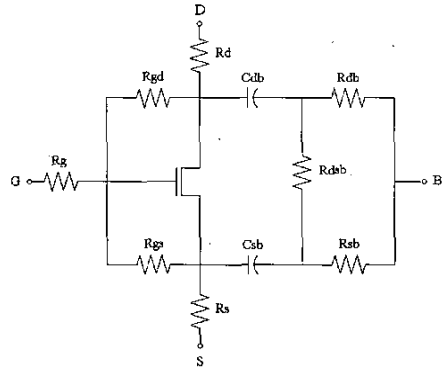

Fig. 1. The equivalent RF circuit for nMOSFETs after BD.

The validity of the modified equivalent RF circuit is verified by the closeness between measured S-parameters data and simulation results obtained from the proposed

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circuit, shown in Fig. 2. It can be used to determine how gate oxide breakdown affects RF circuit operation.

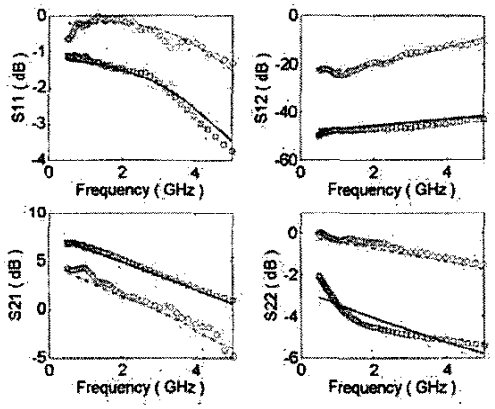

Fig. 2. Measured and simulated S-parameters before and after device breakdown (square: fresh measurement, circle: post-BD measurement, solid line: simulation for fresh device, dash-dot line: simulation for post-BD device).

IV. LNA Performance Analysis

The LNAs evaluated are shown in Fig. 3. One is a common source amplifier (CS LNA), and the other adopts cascode structure. All the devices are composed of 20 fingers with each being 10 μm wide. Both circuits are designed as narrow band LNAs at 1.8 GHz. Source inductive degeneration is used to improve linearity. The inductance at the drain creates a resonant load with the input capacitance of the following mixer stage. Cascode structure minimizes the Miller effect and increases the gain, which is demonstrated by the differences of S12 and S21 between the two circuits, at the expense of increased noise figure.

It should be mentioned that not all fingers experience breakdown simultaneously. Fig. 4 shows noise figures of the CS LNA after up to 3 fingers breakdown. At 1.8 GHz, the noise figure can still meet the general requirement of 2 dB even after 2 fingers breakdown. But IP3 degrades drastically dropping from 0.84 dBm to −13 dBm. Fig. 5 shows the noise figures of the cascode LNA after up to two fingers of input device M1 breakdown. The noise figure degrades more drastically after 2 fingers of M1 have broken down than it does after only 1 finger has broken down. It is concluded that the breakdown of the input device will bring deadly impact on the operation of the cascode LNA. The greater noise figure vulnerability of cascode LNA in comparison to the CS LNA is due to the cascode structure. A wider transistor will lead to a larger noise figure and a greater likelihood that the noise figure will be affected by oxide breakdown.

The degradation of the S-parameters after breakdown is shown in Fig. 6 and Fig. 7 for the CS and cascode LNAs, respectively. The breakdown of only one finger is enough to defunct both LNAs in terms of S-parameters. Among the four S-parameters, S21 seems to be the strongest. It is still greater than generally required 15 dB after one finger breakdowns in both circuits.

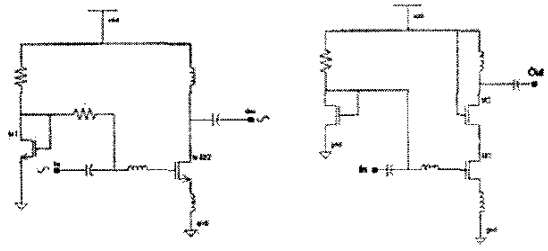

Fig. 3. Schematic of CS LNA (left) and cascode LNA (right).

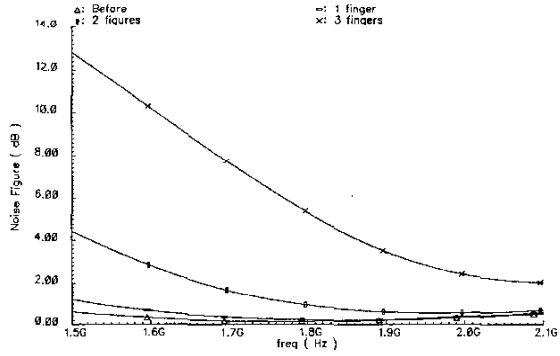

Fig. 4. Noise figures of the CS LNA.

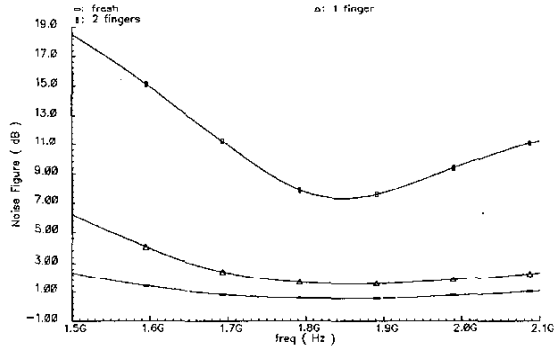

Fig. 5. Change of the noise figures before and after up to 2 fingers of M1 breakdown of the cascode LNA.

However, the breakdown of the cascode device is found to be not as crucial to the operation of the LNA. No matter whether none or one finger of the input device breakdowns, the breakdown of one or several fingers of

the cascode device does not bring more significant damage to the LNA functionality. See Table 1 in [5].

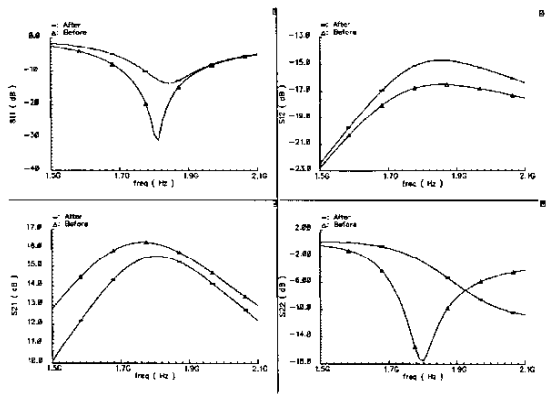

Fig. 6. S-parameters of CS LNA before and after 1 finger breakdowns.

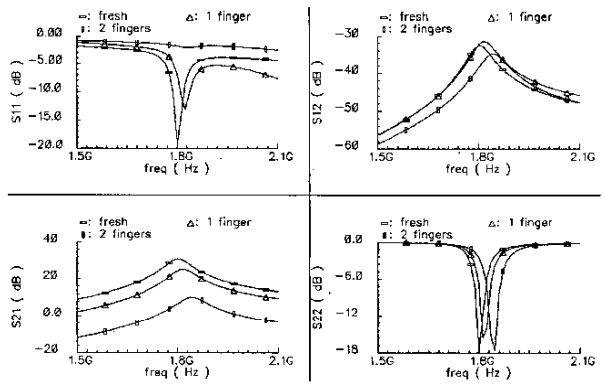

Fig. 7. S-parameters of cascode LNA.

V. Power Amplifier Performance Analysis

The exceedingly high electric fields existing within PA transistors during its operation can easily exceed the breakdown voltages in modern sub-micron technologies. Because of this, PA design in CMOS remains a continuous challenge. For it is known that the portion of the gate oxide near the drain ruptures most frequently in power amplifiers due to the exceedingly high drain voltages [12]. For example, the standard Class-E PA [13] is known to suffer from a maximum drain voltage of $3.57V_{DD}$, therefore making this type of power amplifier a prime candidate for oxide breakdown in the gate to drain region. In this section, the effects of oxide breakdown on PA operation due to high voltage levels are presented.

Fig. 8 displays the Class-E PA used in this analysis. The transistor, M0, has a gate length of 0.16 μm and is composed of 700 fingers each being 10 μm apiece. The circuit was designed to supply 22 dBm of output power at an operating frequency of 950 MHz with a 0.8 V power supply. A finite dc-feed inductor [15] was used instead of an RF choke to help provide some relief on the load resistance and supply voltage. The proposed equivalent RF circuit model in Fig. 1 was inserted into 100 fingers in this design in order to analyze the breakdown effects within the transistor.

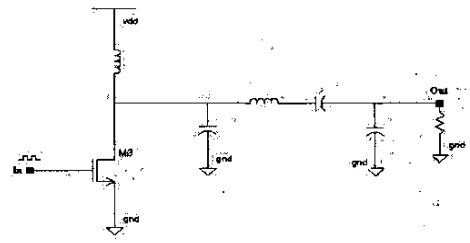

Fig. 8. Class-E power amplifier.

When the power amplifier was simulated using the fresh transistor model files with no breakdown effects included, a drain efficiency (η) of 92% was achieved at the fundamental and held greater than 80% for nearly a 60 MHz bandwidth. After the equivalent RF circuit model and the experimentally generated breakdown model files were applied, the drain efficiency at the fundamental dropped to 73%. Fig. 9 depicts a comparison between the simulated pre-breakdown and post-breakdown drain efficiency values for various frequencies.

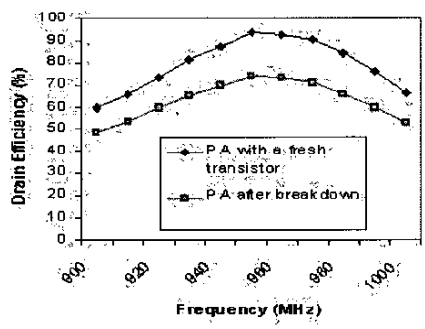

Fig. 9. Drain efficiency versus operation frequency.

One of the main contributors to power loss in a switching mode PA takes place when the nonzero switch voltage and the nonzero switch current overlap, thereby dissipating power through the transistor. As noted in [14], as technology scales down, the "on" resistance across the transistor tends to become a greater problem. Below, in Fig 10, the minimum voltage across the transistor when the transistor is in its conducting stage is displayed for various supply voltages. It was found that following an oxide breakdown, V_{Dmin} increases, thereby causing more

power to be dissipated through the transistor. The change in output power with respect to supply voltage is depicted in Fig. 11. Lastly, Fig. 12 displays how an increase in the number of fingers affected by oxide breakdown leads to an increase in the degradation of the output power.

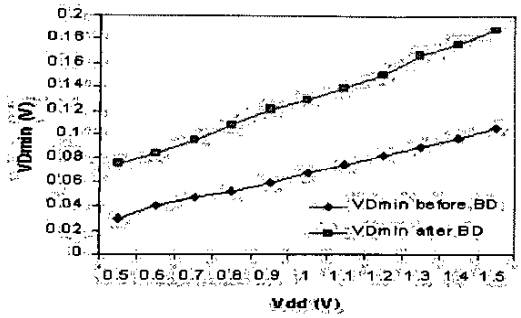

Fig. 10. Vdmin before and after breakdown.

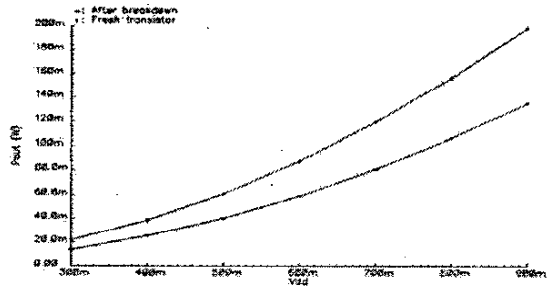

Fig. 11. Output power before and after breakdown.

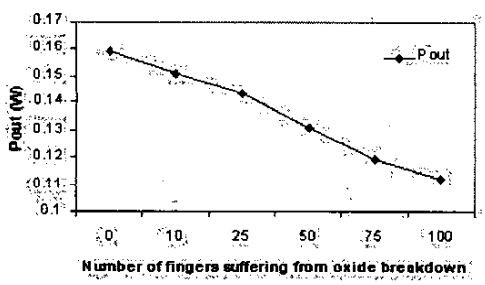

Fig. 12. Decrease in output power with an increase in damaged fingers.

VI. Conclusion

A large degradation in the RF performance of nMOSFETs can be attributed to gate oxide breakdown. For the CS and cascode LNAs, their performances degrade drastically after the input device breakdown. Yet the cascode LNA continues to work even after several fingers in the cascode device have undergone gate oxide breakdown. Cascode LNA is recommended in terms of gate oxide reliability. Oxide breakdown is also shown to dramatically effect the operation of the Class-E power amplifier. The transistor "on" voltage was found to almost double at the assigned supply voltage, therefore indicating an increase in power loss across the transistor. With only one-seventh of the fingers degraded, the drain efficiency and output power were shown to decrease by 20% and 33% at the fundamental frequency, respectively.

References

[1] B. P. Linder, *etc.*, "Gate Oxide Breakdown under Current Limited Constant Voltage Stress," *2000 Symposium on VLSI Technology Dig.*, pp. 214-215, 2000.

[2] Q. Li, J. Zhang, W. Li, J. S. Yuan, Y. Chen, A. S. Oates, "RF Circuit Performance Degradation Due to Soft Breakdown and Hot-Carrier Effect in Deep-Submicrometer CMOS Technology," *IEEE Trans. Microwave Theory and Tech.*, vol. 49, pp. 1546-1551, Sept., 2001.

[3] Q. Li, W. Li, J. Zhang, and J. S. Yuan, "Soft Breakdown and Hot Carrier Reliability of CMOS RF Mixer and Redesign," *2002 IEEE MTT-S Dig.*, pp. 509-512, 2002.

[4] B. Kaczer, "Impact of MOSFET Gate Oxide Breakdown on Digital Circuit Operation and Reliability," *IEEE Trans. Electron Devices*, vol. 49, pp. 500-506, March 2002.

[5] H. Yang, J. S. Yuan, and E. Xiao, "Effect of Gate Oxide Breakdown on RF Device and Circuit Performance," to be published in *IEEE IRPS*, 2003.

[6] W. Liu, *etc.*, "RF MOSFET Modeling Accounting for Distributed Substrate and Channel Resistance with Emphasis on the BSIM3v3 SPICE Model," *IEDM*, pp. 309-312, 1997.

[7] Jia-Jiunn Ou, X. Jin, I. Ma, C. Hu, and P. R. Gray, "CMOS RF Modeling for GHz Communication IC's," *1998 Symposium on VLSI Technology Dig.*, pp. 94-95, 1998.

[8] S. Jen, *etc.*, "Accurate Modeling and Parameter Extraction for MOS Transistors Valid up to 10 GHz," *IEEE Trans. Electron Devices*, vol. 46, pp. 2217-2227, Nov. 1999.

[9] E. Wu, *etc.*, "Structural Dependence of Dielectric Breakdown in Ultra-Thin Gate Oxides and Its Relationship to Soft Breakdown Modes and Device Failure," *IEEE IEDM Tech. Dig.*, pp. 187-190, 1998.

[10] R. Degraeve, *etc.*, "Relation Between Breakdown Mode and Location in Short-Channel nMOSFETs and Its Impact on Reliability Specifications," *IEEE Trans. Device and Materials Reliability*, vol. 1, pp. 163-169, Sept. 2001.

[11] F. Crupi, *etc.*, "Location and Hardness of the Oxide Breakdown in Short Channel n- and p- MOSFETs," *IEEE IRPS*, pp. 55-59, 2002.

[12] Thomas H. Lee, *The Design of Radio Frequency Integrated Circuits*, Cambridge University Press, 1998.

[13] Nathan O. Sokal, Alan D. Sokal, "Class E - A New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers", *IEEE Journal of Solid-State Circuits*, vol. SC-10, no. 3, pp. 168-176, June 1975.

[14] Changsik Yoo, Qiuting Huang, "A Common-Gate Switched 0.9W Class-E Power Amplifier with 41% PAE in 0.25-μm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 36, no. 5, pp. 823-830, May 2001.

[15] C. Chan, K. Toumazou, "Design of a Class E Power Amplifier With Non-Linear Transistor Output Capacitance and Finite DC-Feed Inductance", *IEEE* pp 129-132, 2001.